WHAT IS CLAIMED IS:

1. A semiconductor device comprising a pixel TFT provided in a display region and a driver circuit TFT provided around said display region over a same substrate, wherein:

said pixel TFT and said driver circuit TFT comprise gate electrodes formed from a first conductive layer, said gate electrodes are in electrical contact through connectors with gate wirings formed from a second conductive layer, and said connectors are provided outside channel-forming regions of said pixel TFT and said driver circuit TFT.

2. A semiconductor device according to claim 1, wherein a storage capacitor is formed in said display region by a semiconductor layer connected to a source or a drain region of said pixel TFT and contains a single conductive impurity element, a capacitor wiring and an insulating film between said semiconductor layer and said capacitor wiring, and wherein said capacitor wiring is formed by said first conductive layer and said second conductive layer.

Sub A1 3. A semiconductor device according to claim 1, wherein said first conductive layer is composed mainly of at least one selected from Ta, W, Ti and Mo, and said second conductive layer is composed mainly of Al or Cu.

4. A semiconductor device according to claim 1, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A)

Sub A' Cont

and composed mainly of at least one selected from Ta, W, Ti and Mo, and a conductive layer (C) formed on regions where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti and Mo, and

wherein said second conductive layer comprises a conductive layer (D) composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo.

5. A semiconductor device according to claim 4, wherein said conductive layer (B) contains argon as an added element, and an oxygen concentration in said conductive layer (B) is 30 ppm or less.

Sub A2

6. A semiconductor device according to claim 1, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A) and composed mainly of at least one selected from Ta, W, Ti and Mo and a conductive layer (C) formed on regions where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti and Mo,

wherein said second conductive layer comprises a conductive layer (D) composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo, and

wherein said conductive layer (C) and said conductive layer (D) are in contact at said connectors.

7. A semiconductor device according to claim 6, wherein said conductive layer (B) contains argon as an added element, and an oxygen concentration in said conductive layer (B) is 30 ppm or less.

8. A semiconductor device according to claim 1, wherein said semiconductor device is an EL display device.

9. A semiconductor device according to claim 1, wherein said semiconductor device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera and a digital video disk player.

10. A semiconductor device having a pixel TFT provided in a display region and a driver circuit TFT provided around said display region over a same substrate, said semiconductor device comprising:

said pixel TFT comprising at least one lightly doped region disposed so as not to overlap said gate electrode of said pixel TFT;

first n-channel TFT of said driver circuit comprising at least one lightly doped region disposed so as to overlap said gate electrode of said first n-channel TFT;

second n-channel TFT of said driver circuit comprising at least one lightly doped region disposed so that at least a portion thereof overlaps said gate electrode of said second n-channel TFT; and

gate electrodes of said pixel TFT and said driver circuit TFT formed from a first conductive layer,

wherein said gate electrodes are in electrical contact with gate wirings formed

from a second conductive layer through connectors provided outside channel-forming regions of said pixel TFT and said driver circuit TFT.

11. A semiconductor device according to claim 10, wherein a storage capacitor is formed in said display region by a semiconductor layer connected to a source or a drain region of said pixel TFT and contains a single conductive impurity element, a capacitor wiring and an insulating film between said semiconductor layer and said capacitor wiring, and wherein said capacitor wiring is formed by said first conductive layer and said second conductive layer.

Sub A3

12. A semiconductor device according to claim 10, wherein said first conductive layer is composed mainly of at least one selected from Ta, W, Ti and Mo, and said second conductive layer is composed mainly of Al or Cu.

13. A semiconductor device according to claim 10, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A) and composed mainly of at least one selected from Ta, W, Ti and Mo, and a conductive layer (C) formed on regions where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti and Mo, and

wherein said second conductive layer comprises a conductive layer (D) composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo.

14. A semiconductor device according to claim 13, wherein said conductive layer (B) contains argon as an added element, and an oxygen concentration in said conductive layer (B) is 30 ppm or less.

Sub A4

15. A semiconductor device according to claim 10, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A) and composed mainly of at least one selected from Ta, W, Ti and Mo and a conductive layer (C) formed on regions where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti and Mo, and

wherein said second conductive layer comprises a conductive layer (D) composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo, and

wherein said conductive layer (C) and said conductive layer (D) are in contact at said connectors.

16. A semiconductor device according to claim 15, wherein said conductive layer (B) contains argon as an added element, and an oxygen concentration in said conductive layer (B) is 30 ppm or less.

17. A semiconductor device according to claim 10, wherein said semiconductor device is an EL display device.

18. A semiconductor device according to claim 10, wherein said semiconductor

device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera and a digital video disk player.

19. A semiconductor device having a display region and a driver circuit provided around said display region over a same substrate, said semiconductor device comprising:

said display region comprising a pixel TFT provided with a lightly doped region not overlapping a gate electrode of said pixel TFT; and

said driver circuit comprising at least a first n-channel TFT provided with a whole lightly doped region overlapping a gate electrode of said first n-channel TFT and a second n-channel TFT provided with a portion of a lightly doped region overlapping a gate electrode of said second n-channel TFT,

wherein at least said gate electrodes of said pixel TFTs and said first and second n-channel TFTs are formed from a first conductive layer, and gate wirings connected to said gate electrodes are formed from a second conductive layer, and

wherein said gate electrodes and said gate wirings are electrically connected through connectors outside channel-forming regions of said pixel TFT and said driver circuit TFT.

20. A semiconductor device according to claim 19, wherein a storage capacitor is formed in said display region by a semiconductor layer connected to a source or a drain region of said pixel TFT and contains a single conductive impurity element, a capacitor wiring and an insulating film between said semiconductor layer and said capacitor wiring, and wherein said capacitor wiring is formed by said first conductive

layer and said second conductive layer.

Sub A5

21. A semiconductor device according to claim 19, wherein said first conductive layer is composed mainly of at least one selected from Ta, W, Ti and Mo, and said second conductive layer is composed mainly of Al or Cu.

22. A semiconductor device according to claim 19, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A) and composed mainly of at least one selected from Ta, W, Ti and Mo, and a conductive layer (C) formed on regions where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti and Mo, and

wherein said second conductive layer comprises a conductive layer (D) composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo.

23. A semiconductor device according to claim 22, wherein said conductive layer (B) contains argon as an added element, and an oxygen concentration in said conductive layer (B) is 30 ppm or less.

Sub A6

24. A semiconductor device according to claim 19, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A) and composed mainly of at least one selected from Ta, W, Ti and Mo and a

conductive layer (C) formed on regions where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti and Mo,

wherein said second conductive layer comprises a conductive layer (D) composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo, and

wherein said conductive layer (C) and said conductive layer (D) are in contact at said connectors.

25. A semiconductor device according to claim 24, wherein said conductive layer (B) contains argon as an added element, and an oxygen concentration in said conductive layer (B) is 30 ppm or less.

26. A semiconductor device according to claim 19, wherein said semiconductor device is an EL display device.

27. A semiconductor device according to claim 19, wherein said semiconductor device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera and a digital video disk player.

28. A method for fabricating a semiconductor device having a pixel TFT provided in a display region and a driver circuit TFT provided around said display region over a same substrate, said method comprising the steps of:

forming gate electrodes of said pixel TFT and said driver circuit TFT from a

first conductive layer; and

forming gate wirings connected to said gate electrodes from a second conductive layer,

wherein said gate electrodes and said gate wirings are connected through connectors provided outside channel-forming regions of said pixel TFT and said driver circuit TFT.

29. A method according to claim 28, wherein said first conductive layer is formed mainly of at least one selected from Ta, W, Ti and Mo, and said second conductive layer is formed mainly of Al or Cu.

30. A method according to claim 28, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A) and composed mainly of at least one selected from Ta, W, Ti and Mo, and a conductive layer (C) formed on areas where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti and Mo, and

wherein said second conductive layer comprises a conductive layer (D) composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo.

31. A method according to claim 30, wherein said conductive layer (A) is formed by a sputtering method using a target composed mainly of at least one selected from Ta, W, Ti and Mo, in a mixed atmosphere of argon and nitrogen or ammonia.

32. A method according to claim 30, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen atmosphere with oxygen at a concentration of 1 ppm or less.

33. A method according to claim 30, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen plasma atmosphere with oxygen at a concentration of 1 ppm or less.

34. A method according to claim 28, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A) and composed mainly of at least one selected from Ta, W, Ti and Mo, and a conductive layer (C) formed on areas where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti and Mo,

wherein said second conductive layer comprises a conductive layer (D) composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo, and

wherein said conductive layer (C) and said conductive layer (D) are in contact at said connector.

35. A method according to claim 34, wherein said conductive layer (A) is formed by a sputtering method using a target composed mainly of at least one selected from Ta, W, Ti and Mo, in a mixed atmosphere of argon and nitrogen or ammonia.

36. A method according to claim 34, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen atmosphere with oxygen at a concentration of 1 ppm or less.

37. A method according to claim 34, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen plasma atmosphere with oxygen at a concentration of 1 ppm or less.

38. A method according to claim 28, wherein said semiconductor device is an EL display device.

39. A method according to claim 28, wherein said semiconductor device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera and a digital video disk player.

40. A method for fabricating a semiconductor device having a pixel TFT provided in a display region and a driver circuit TFT provided around said display region over a same substrate, said method comprising the steps of:

selectively introducing an n-type impurity element to semiconductor layers of first and second n-channel TFTs of said driver circuit at a concentration of 2×10^{16} to 5×10^{19} atoms/cm^3;

forming gate electrodes of said pixel TFT and said driver circuit TFT from a first conductive layer;

selectively introducing a p-type impurity element to a semiconductor layer of

p-channel TFT of said driver circuit at a concentration of 3×10^{20} to 3×10^{21} atoms/cm^3;

selectively introducing an n-type impurity element to said semiconductor layers of said first and said second n-channel TFT of said driver circuit and said semiconductor layer of said pixel TFT at a concentration of 1×10^{20} to 1×10^{21} atoms/cm^3;

selectively introducing an n-type impurity element to the semiconductor layer of said pixel TFT to a concentration range of 1×10^{16} to 5×10^{18} atoms/cm^3, using at least said gate electrode of said n-channel TFT as a mask; and

forming gate wirings of said pixel TFT and said driver circuit TFT from a second conductive layer;

wherein said gate electrodes and said gate wirings are connected through connectors provided outside channel-forming regions of said pixel TFT and said driver circuit TFT.

41. A method according to claim 40, wherein said first conductive layer is formed mainly of at least one selected from Ta, W, Ti and Mo, and said second conductive layer is formed mainly of Al or Cu.

42. A method according to claim 40, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A) and composed mainly of at least one selected from Ta, W, Ti and Mo, and a conductive layer (C) formed on areas where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti

and Mo, and

wherein said second conductive layer comprises a conductive layer (D) composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo.

43. A method according to claim 42, wherein said conductive layer (A) is formed by a sputtering method using a target composed mainly of at least one selected from Ta, W, Ti and Mo, in a mixed atmosphere of argon and nitrogen or ammonia.

44. A method according to claim 42, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen atmosphere with oxygen at a concentration of 1 ppm or less.

45. A method according to claim 42, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen plasma atmosphere with oxygen at a concentration of 1 ppm or less.

46. A method according to claim 40, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A) and composed mainly of at least one selected from Ta, W, Ti and Mo, and a conductive layer (C) formed on areas where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti and Mo,

wherein said second conductive layer comprises a conductive layer (D)

composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo, and

wherein said conductive layer (C) and said conductive layer (D) are in contact at said connector.

47. A method according to claim 46, wherein said conductive layer (A) is formed by a sputtering method using a target composed mainly of at least one selected from Ta, W, Ti and Mo, in a mixed atmosphere of argon and nitrogen or ammonia.

48. A method according to claim 46, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen atmosphere with oxygen at a concentration of 1 ppm or less.

49. A method according to claim 46, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen plasma atmosphere with oxygen at a concentration of 1 ppm or less.

50. A method according to claim 40, wherein said semiconductor device is an EL display device.

51. A method according to claim 40, wherein said semiconductor device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera and a digital video disk player.

52. A method for fabricating a semiconductor device having a pixel TFT

provided in a display region and a driver circuit TFT provided around said display region over a same substrate, said method comprising the steps of:

selectively introducing an n-type impurity element to semiconductor layers of first and second n-channel TFTs of said driver circuit and to a semiconductor layer of a storage capacitor in said display region at a concentration of 2×10^{16} to 5×10^{19} atoms/cm^3;

forming gate electrodes of said pixel TFT and said driver circuit TFT from a first conductive layer;

selectively introducing a p-type impurity element to a semiconductor layer of p-channel TFT of said driver circuit at a concentration of 3×10^{20} to 3×10^{21} atoms/cm^3;

selectively introducing an n-type impurity element to said semiconductor layers of said first and second n-channel TFT of said driver circuit and to said semiconductor layer of said pixel TFT at a concentration of 1×10^{20} to 1×10^{21} atoms/cm^3;

selectively introducing an n-type impurity element to said semiconductor layer of said pixel TFT at a concentration of 1×10^{16} to 5×10^{18} atoms/cm^3, using at least said gate electrode of said n-channel TFT as a mask; and

forming gate wirings of said pixel TFT and said driver circuit TFT from a second conductive layer,

wherein said gate electrodes and said gate wirings are connected through connectors provided outside channel-forming regions of said pixel TFT and said driver circuit TFT.

53. A method according to claim 52, wherein said first conductive layer is

formed mainly of at least one selected from Ta, W, Ti and Mo, and said second conductive layer is formed mainly of Al or Cu.

54. A method according to claim 52, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A) and composed mainly of at least one selected from Ta, W, Ti and Mo, and a conductive layer (C) formed on areas where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti and Mo, and

wherein said second conductive layer comprises a conductive layer (D) composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo.

55. A method according to claim 54, wherein said conductive layer (A) is formed by a sputtering method using a target composed mainly of at least one selected from Ta, W, Ti and Mo, in a mixed atmosphere of argon and nitrogen or ammonia.

56. A method according to claim 54, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen atmosphere with oxygen at a concentration of 1 ppm or less.

57. A method according to claim 54, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen plasma atmosphere with oxygen at a concentration of 1 ppm or less.

58. A method according to claim 52, wherein said first conductive layer comprises a conductive layer (A) containing nitrogen and at least one selected from Ta, W, Ti and Mo, a conductive layer (B) formed on said conductive layer (A) and composed mainly of at least one selected from Ta, W, Ti and Mo, and a conductive layer (C) formed on areas where said conductive layer (B) does not contact said conductive layer (A) and containing nitrogen and at least one selected from Ta, W, Ti and Mo,

wherein said second conductive layer comprises a conductive layer (D) composed mainly of Al or Cu and a conductive layer (E) composed mainly of at least one selected from Ta, W, Ti and Mo, and

wherein said conductive layer (C) and said conductive layer (D) are in contact at said connector.

59. A method according to claim 58, wherein said conductive layer (A) is formed by a sputtering method using a target composed mainly of at least one selected from Ta, W, Ti and Mo, in a mixed atmosphere of argon and nitrogen or ammonia.

60. A method according to claim 58, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen atmosphere with oxygen at a concentration of 1 ppm or less.

61. A method according to claim 58, wherein said conductive layer (C) is formed by heat treating of said conductive layer (B) in a nitrogen plasma atmosphere with oxygen at a concentration of 1 ppm or less.

62. A method according to claim 52, wherein said semiconductor device is an EL display device.

63. A method according to claim 52, wherein said semiconductor device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera and a digital video disk player.